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10/083,814	02/27/2002	Joseph Francis Mann	01AB162	6548

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/083,814	MANN ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A.SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,8-16 and 18-23* is/are rejected.

7)☒ Claim(s) *7 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 5 and 16 are objected to because of the following informalities: "external random access memory" cannot include "non-volatile memory". Appropriate correction is required.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 10-16, 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fullam et al., US Patent 5802550, hereinafter Fullam, in view of Gupta, US Patent 6577158.

4. In re claim 1, Fullam discloses an integrated processor system [fig.3] comprising:

- A common integrated circuit substrate [col.6, ll.60-63] without general-purpose random access memory [col.6, l.46, l.59; register 54 and cache units do not constitute general purpose random access memory according to Applicant's Remarks dated July 11, 2007] and holding each of:
    - A processing unit for performing arithmetic and logical operations [52].
    - At least one internal system storage structure selected from the group consisting of caches [25, 27; col.6, l.59], buffers, and registers [54].
    - An external memory interface [col.6, ll.55-57] for connecting to an external random access memory [58] not on the common substrate [col.1, ll.33-34; slow speed RAM as peripheral memory device 58].

- Wherein the processing unit [52]:
    - (i) Executes at least a portion of a bootstrap program [boot process] to determine memory setup data [e.g., speed configuration data associated with different external memory] needed to communicate with external random access memory while using the at least one internal system storage structure for temporary storage required for execution of the bootstrap program without write access to external random access memory for storage of data necessary for the execution of the bootstrap program [fig.1b; col.3, l.2 – col.4, l.1; bidirectional caches used for execution without need to write to external memory].
    - (ii) Only after the execution of (i) connects to the external random access memory using the determined set up data for the reading and writing to the external random access memory [col.4, ll.19-21; col.7, l.27 – col.8, l.6; e.g., high speed data with particular cycles related to wait time would not work with "slow" external memory].

5. Fullam did not disclose explicitly the bootstrap program is stored in a bootstrap memory also on the common integrated circuit substrate.

6. Gupta discloses an integrated processor system [fig.1] comprising a common integrated circuit substrate [105] holding a bootstrap memory [140] communicating with the processing unit [130] and holding a bootstrap [startup] program executable by the processing unit [fig.1; col.5, ll.20-31].

7. It would have been obvious to one of ordinary skill in the art, having the teachings of Fullam and Gupta before him at the time the invention was made, to modify the integrated

processor system taught by Fullam to include the teachings of Gupta, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it reduces the size and power consumption as well as manufacturing costs [Gupta: col.1, ll.27-38].

8. In re claims 2 and 13, Gupta discloses interface circuits [e.g., 120] for communicating electrical signals [e.g., video signals] with non-memory external devices [e.g., DVD player] [col.5, ll.2-15].

9. It would have been obvious to one of ordinary skill in the art, having the teachings of Fullam and Gupta before him at the time the invention was made, to modify the integrated processor system taught by Fullam to include the well known teachings of Gupta, as the use of non-memory external devices is very well known and suitable for use with the integrated circuit of Fullam. One of ordinary skill in the art would have been motivated to make such a combination as it provides a well known way to expand an integrated circuit's peripheral functions.

10. As to claims 3 and 14, Fullam discloses a memory interface [56] for communicating with external random access memory [58] and wherein the processing unit [52] executes at least a portion of the bootstrap program [boot process] to provide for the acquisition of external memory setup data [default from 54] required for the memory interface to initiate communication with external random access memory [col.7, ll.39-50].

11. As to claims 4 and 15, Fullam discloses, a network interface and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of the

external memory setup data through a network connection [col.7, ll.39-50; configuration data stored in external 64 accessed through network].

12. As to claims 5 and 16, Fullam discloses, wherein the external memory includes non-volatile memory [64] and volatile memory [58] and wherein the processing unit executes at least a portion of the bootstrap program to provide for the acquisition of the external memory setup data for the external volatile memory from the external non-volatile memory [col.3, ll.59-63; col.7, ll.39-50].

13. As to claim 6, Fullam discloses, comprising wherein the external non-volatile memory is flash memory [col.7, ll.41-42].

14. As to claims 10 and 20, Fullam discloses, wherein the processing unit further executes at least a portion of the bootstrap program to store the memory setup data in the memory interface [54 part of 56] and then to execute a program contained in external random access memory [col.1, ll.25-50; col.7, l.38 – col.8, l.19].

15. As to claims 11 and 21, Fullam discloses, wherein the memory setup data is selected from the group consisting of: memory type as static or dynamic, memory speed, memory size, memory parity, and memory timing [col.3, ll.47-58; col.7, ll.11-26; col.9, ll.5-7].

16. In re claim 12, Fullam discloses, a method of initializing an integrated processor system not including a common integrated circuit substrate general-purpose random access memory [col.6, l.46, l.59; register 54 and cache units do not constitute general purpose random access memory according to Applicant's Remarks dated July 11, 2007] but including on the common integrated circuit substrate [col.6, ll.60-63], a processing unit for performing arithmetic and logical operations [52]; at least one internal system storage structure selected from the group

consisting of: caches [25, 27; col.6, l.59], buffers, and registers [54]; and an external memory interface [col.6, ll.55-57] for connecting to an external general purpose random access memory not on the common substrate [col.1, ll.33-34; slow speed RAM as peripheral memory device 58] comprising the step of:

- Executing at least a portion of a bootstrap program [boot process] by the processing unit to determine memory set-up data [e.g., speed configuration data associated with different external memory] needed to communicate with different type of external memory while using the at least one internal system storage structure for temporary storage needed for the execution of the bootstrap program without access to external memory for storage of data needed for the execution of the bootstrap program [caches used for execution] [col.3, l.2 – col.4, l.1; col.7, ll.51-53].
- Only after determination of the memory set-up data, connecting to the external memory using the determined set up data for the reading and writing to the external memory [col.7, l.27 – col.8, l.6; e.g., high speed data with particular cycles related to wait time would not work with "slow" external memory].

17. As to claims 22 and 23, Gupta discloses an integrated processor system [fig.1] wherein the bootstrap [startup] program is stored in a bootstrap memory [140] also on the common integrated circuit substrate [105] [col.5, ll.20-31].

18. Claims 8 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fullam and Gupta as applied to claims 1 and 12 above, and further in view of Devereux, US Patent 6671779.

19. In re claims 8 and 18, Fullam and Gupta taught each and every limitation as discussed above. Fullam and Gupta discloses the integrated processor system wherein the system storage structure is a cache memory [54] and wherein the processing unit executes at least a portion of the bootstrap program to read arbitrary data into the cache memory [col.7, ll.39-50]. Fullam and Gupta did not disclose locking the cache memory against further reading or writing to external memory.

20. Devereux discloses an integrated processor system [fig.3] wherein the system storage structure is a cache memory [30'] and wherein the processing unit [10] executes at least a portion of the bootstrap program to read arbitrary data [data values for interrupts] into the cache memory and then to lock the cache memory against further reading or writing to external memory [80] so that it may be used as variable storage for further execution of the bootstrap program [col.7, ll.36-49; external memory capable of being used as variable storage for execution of the bootstrap program].

21. It would have been obvious to one of ordinary skill in the art, having the teachings of Devereux, Fullam and Gupta before him at the time the invention was made, to modify the integrated processor system taught by Fullam and Gupta to include the teachings of Devereux, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it provides speed benefits without data corruption [Devereux: col.7, ll.36-49].

22. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fullam and Gupta as applied to claims 3 and 14 above, and further in view of Little et al., US Patent 6272637, hereinafter Little.

23. In re claims 9 and 19, Fullam and Gupta taught each and every limitation of the claim, as discussed above in reference to claim 3. Fullam and Gupta discloses wherein the processing unit executes at least a portion of the bootstrap program to store the memory setup data in the memory interface [54 part of 56] [col.1, ll.25-50; col.7, l.38 – col.8, l.19]. Fullam and Gupta did not disclose explicitly loading additional programs for execution into external memory.

24. Little discloses an integrated processor system [fig.3] wherein the processing unit loads additional programs for execution into external memory [130] [col.5, ll.39-51].

25. It would have been obvious to one of ordinary skill in the art, having the teachings of Little, Fullam and Gupta before him at the time the invention was made, to modify the integrated processor system taught by Fullam and Gupta to include the teachings of Little, in order to obtain the claimed integrated processor system. One of ordinary skill in the art would have been motivated to make such a combination as it provides secured processing of information [Little: col.1, ll.39-59].

Allowable Subject Matter

26. Claims 7 and 17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

27. The following is a statement of reasons for the indication of allowable subject matter: the claims are allowable because none of the references cited, either alone or in combination discloses or renders obvious an integrated processor system of claims 7 and 17, wherein "the processing unit includes an address translation table... at least a portion of the bootstrap program

to make a temporary address translation table in a buffer memory so as to make the cache memory available for temporary storage".

Response to Arguments

28. Applicant's arguments filed July 11, 2007 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Tse Chen
July 26, 2007